

ECE 85L Digital Logic Design Laboratory
Fresno State, Lyles College of Engineering
Electrical and Computer Engineering Department
Spring 2015

Laboratory 4 – LOGIC GATE DYNAMIC CHARACTERISTICS

1. OBJECTIVES

- Review the operation of an Oscilloscope
- Measure the Rise Time and Fall Time of a waveform.
- Measure the Propagation Delay of a typical Logic Gate.
- Develop an understanding for circuits that operate only as a result of Propagation Delay.

2. DISCUSSION

Although this is a course in Digital Logic, there are a few analog parameters that affect the design and operation of such circuits. Three of the more important of these parameters are Rise Time, Fall Time, and Propagation Delay.

The Propagation Delay times T_{PLH} (Low to High) and T_{PHL} (High to Low) are the time intervals between the appearance of a sufficient change in the input to switch a gate and the appearance of a sufficient change in the output of that gate to switch the following gate. Propagation delay is measured between the time that the input has reached 50% of its maximum (or minimum) value and the time that the output has reached 50% of its maximum (or minimum) value. In the example below, for which the device is an inverter, the propagation delay would be the time between the point at which the input reaches 2.5 V (50% of the difference between the minimum of 0 V and the maximum of 5 V) and the point at which the output reaches 2.5 V.

As the propagation delay corresponding to a Low-to-High output change may be (and usually is) different from that corresponding to a High-to-Low output change, each must be specified separately.

$T_{PD} = 1/2 (T_{PLH} + T_{PHL})$ is defined as the average propagation delay time.

Switching Times

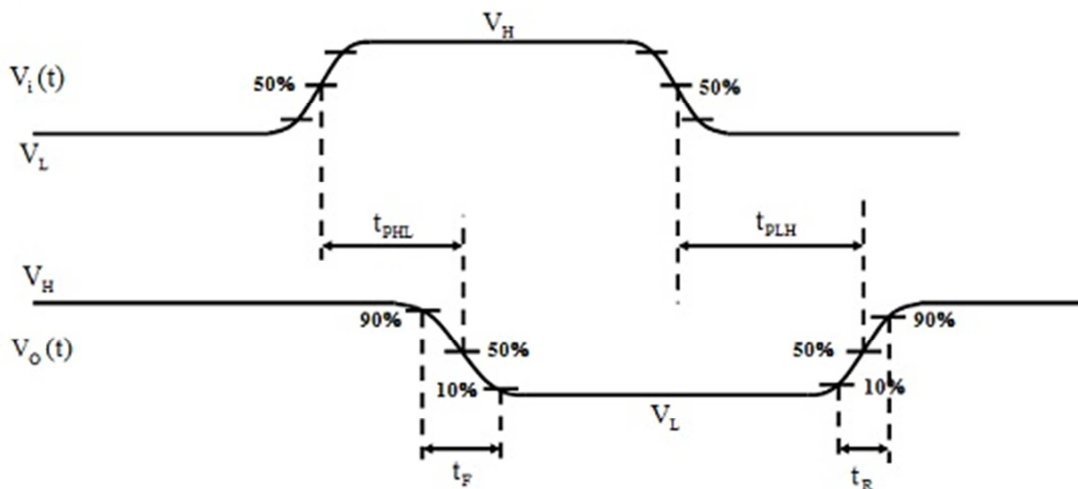


Figure 2.1: Definitions of Propagation Delay Times T_{PLH} and T_{PHL} , and Rise and Fall Times T_R and T_F .

Values for the propagation delay components may be found in manufacturer's data sheets.

The other two parameters, Rise Time T_R and Fall Time T_F , relate to the speed at which a waveform changes from its Low State to its High State (Rise Time) or from its High State to its Low State (Fall Time). Rise Time is measured from the 10% point to the 90% point, while Fall Time is measured from the 90% point to the 10% point (see Figure 2.1). With a High of 5 V and a low of 0 V, the 10% point is at 0.5 V while the 90% point is at 4.5 V.

3. PRELAB

1. One way to measure the average propagation delay time of a gate is to connect an odd number of identical gates in a closed loop, which will then oscillate. The time required for a signal to pass around the loop will be the sum of all the T_{PLH} and T_{PHL} of the gates in the loop. The low-to high transition is called the Leading Edge; the high-to low transition is called the Trailing Edge or Falling Edge.

Prove to yourself that the circuit shown below is unstable (oscillates) by arbitrarily assigning to one of the inputs (i.e., A) one of the two possible Logic levels (i.e., HIGH = Logic Level 1). With this assignment determine, in order, the resulting Logic levels for B, C, and again A around the loop. Follow this reasoning to prove that neither arbitrarily assigned level (0 or 1) is stable.

Derive a formula for the period T of the signal generated by the oscillating loop as a function of T_{PD} (assuming all inverters have identical delays) and **zero Rise and Fall Times** by completing a timing diagram for the loop.

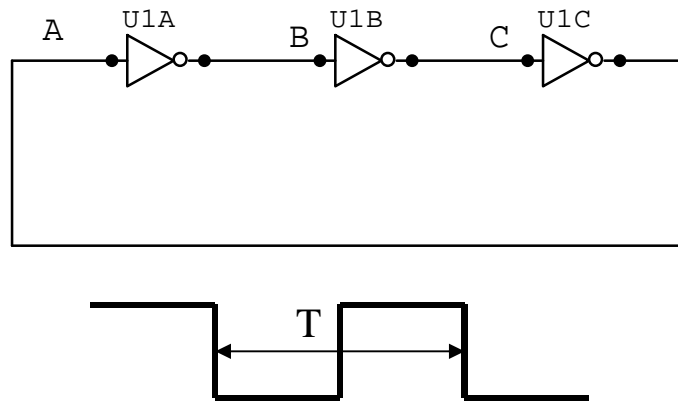


Figure 3.1: Unstable circuit using an odd number of NOT Gates.

Derive a formula for the frequency F ($F=1/T$) of the signal generated by the oscillating loop. A portion of the timing diagram from which the formula for T is to be derived is shown in Figure 3.2. Since circuit oscillates, we can (arbitrarily) start the timing diagram just before one of the leading edges of the input to inverter A. The output of B will change one (High-to-Low) Propagation Delay T_{PHL} after this (leading) edge of A; the output of C will change one (Low-to-High) Propagation Delay T_{PLH} after this (trailing) edge of B, and so on.

Using Multisim, produce a schematic diagram corresponding to Figure 3.1. Use the 7404 for all inverters. Follow the guidelines of Laboratory 2 in developing your diagram.

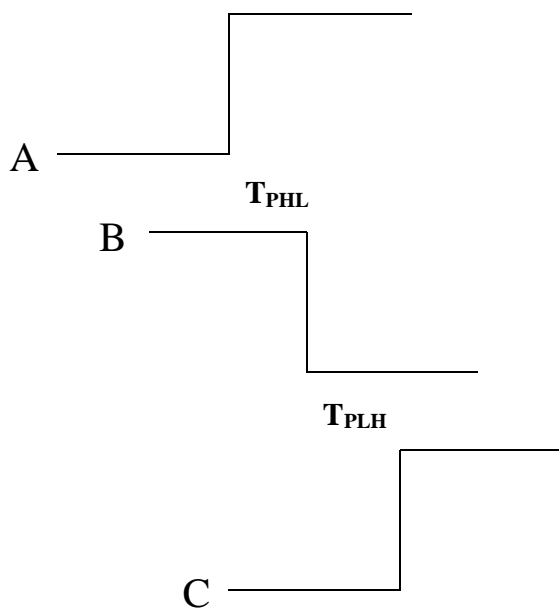


Figure 3.2: Start of Timing Diagram for Calculation of T_{PD} and Period T (or Frequency F).

2. Look up the type "00" NAND and type "86" XOR gates in Data Sheets and record the expected range of switching times (Low-to-High and High-to-Low). Note that the times for a particular chip vary depending on the fabrication technique, packaging, etc. Most of the ICs used in the lab are SN74XX in type N packages.
3. The Dual Edge Detector Circuit shown in Figure 3.3 operates only because of propagation delay. Create a timing diagram showing the output of the circuit. Assume the input is (one half cycle of) a square wave whose period is long compared to the rise and fall times. All gates are assumed to have identical propagation delays T_{PD} and 0 ns Rise and Fall Times T_R and T_F . The initial condition of the output of each of the three gates (0 or 1) is given to assist you in this process.

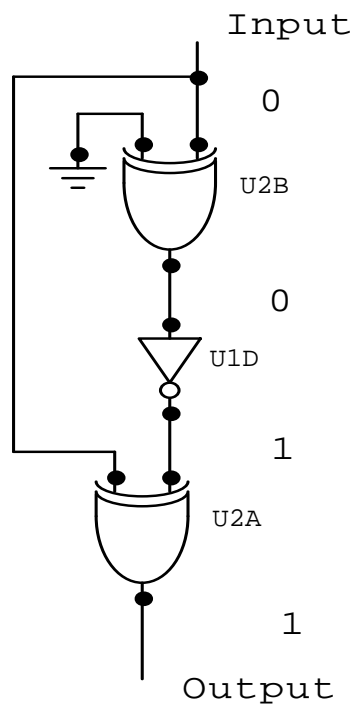


Figure 3.3: Dual Edge Detector Circuit

4. LAB ASSIGNMENT

The primary objective of this lab is to understand and measure the dynamic characteristics of gates (those that are time-dependent). The appropriate test vehicle for such characteristics is the Oscilloscope.

1. Set the Function Generator controls to produce a 0-5 V square wave output with a frequency of 100 kHz. Measure the Rise and Fall Times of this waveform (the

X10 Time Base Expansion feature of the Oscilloscope will help you in this measurement). Draw the leading and trailing edges of this waveform, as observed on the oscilloscope.

CAUTION: Chips may be damaged by driving them with the wrong Function Generator Output. Make sure the output of the Function Generator 0-5 V before proceeding to step 2. This is best measured using the Oscilloscope.

2. With the Function Generator controls set as in Part 1 above, connect two NAND Gates of a 7400 chip as inverters, as shown in Figure 4.1:

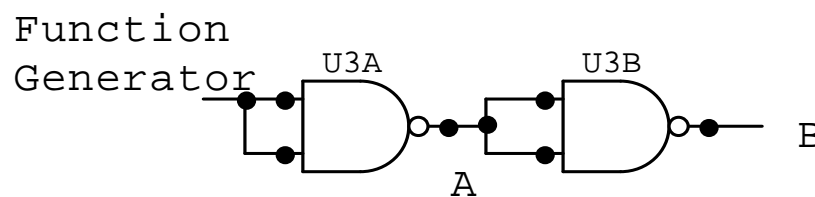


Figure 4.1: Cascaded NAND Gates as Inverters

Observe simultaneously the leading edge of A and the resulting trailing edge of B on the Oscilloscope using both channels. Sketch both waveforms. Measure and record the Propagation Delay at this edge. Then observe the trailing edge of A and the resulting leading edge of B on the oscilloscope. Sketch both waveforms. Measure and record the Propagation Delay at this edge. Insert a short length of wire at point A and physically grasp the unconnected end tightly with your fingers; observe the effect on waveform A. Can you explain this phenomenon?

3. The circuit in Figure 4.2 interconnects NAND gates A, B, C in an Oscillating Ring, under the assumption that each gate has Propagation Delay Time T_{PD} and 0 ns Rise and Fall times T_R and T_F .

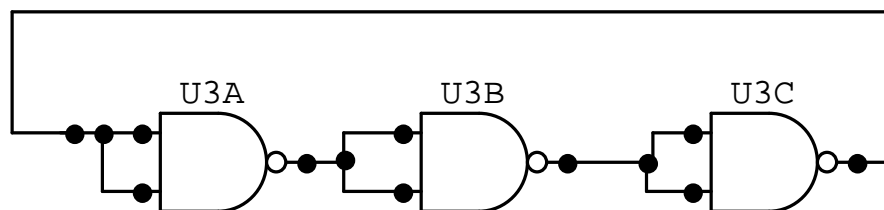


Figure 4.2: Oscillating Ring Circuit using Cascaded NAND Gates

This circuit is functionally identical to that which you analyzed in Prelab. From the specifications in the TTL data sheet for a Type SN7400N NAND Gate using the "typical" values, calculate the average expected propagation delay time:

$$T_{PD} = 1/2 (T_{PLH} + T_{PHL})$$

From T_{PD} , calculate the expected period T and expected frequency F of the circuit.

Connect 3 Type 00 NAND gates to form an oscillating ring. Note that the circuit is an oscillator and that other than power, it requires no input. Observe the output on the Oscilloscope. Primarily due to non-zero Rise and Fall times, the output differs considerably from that of an ideal square wave. Sketch the output of one of the NAND gates and measure the waveform's period with the Oscilloscope. How does this measurement compare with your calculated value? What is the frequency F ($f = 1/T$) of the output signal? How does it compare with your calculation?

4. The circuit shown in Figure 4.3 is the "Dual Edge Detector" recommended by FAIRCHILD'S APPLICATIONS HANDBOOK.

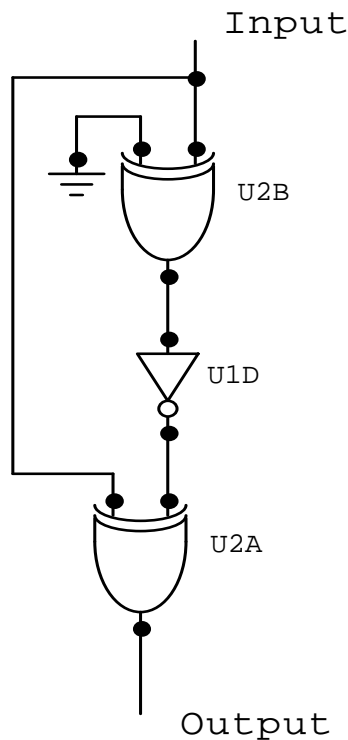


Figure 4.3: Dual Edge Detector Circuit

This circuit is identical to the one examined in Prelab.

Using the 7486 chip, set up the above circuit using XOR Gates on a single chip. Fabricate the inverter with an XOR gate with one input tied HIGH. Drive your circuit with a 1 MHz

Square-Wave from the Function Generator, and observe and sketch both input and output from the Oscilloscope. Note that the outputs may be "spikey" rather than square because of the non-zero Rise and Fall Times.

5. REVIEW QUESTIONS

1. Based on your observations, would you expect the Rise and Fall Times of (the output of) a gate to be identical?
2. Would you expect the Propagation Delay of multiple gates on the same chip to be identical? Why or why not?
3. Why are Rise time and Fall Times measured from 10 to 90% Voltage values rather than 0 to 100%?
4. What are the relationships between Rise/Fall Times and Leading/Trailing waveform edges?
5. How does the addition of stray capacitance (such as touching a circuit with your fingers) affect the Rise Time or Fall Time of that waveform?