ECE 85L Digital Logic Design Laboratory

Fresno State, Lyles College of Engineering
Electrical and Computer Engineering Department
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Laboratory 12 – Registers

1. OBJECTIVES

- Understand the Basics of a Register
- Fabricate and Test a 4-Stage Serial-In Serial-Out Shift Register
- Fabricate and Test a 4-State Bi-Directional Serial-In Serial-Out Shift Register

2. DISCUSSION

Indigenous to all computation is the storage and retrieval of information. Since the computer manipulates information in binary form, all information must be represented in binary. A single location capable of storing only a single 1 or 0 is called a bit. Such locations can be grouped together for manipulation as a nibble (four contiguous bits), a byte (eight contiguous bits) etc. A circuit that is capable of holding ***N*** such bits for storage and manipulation is called an ***N***-bit Register.

As shown in Figure 2.1, the J-K Flip-Flop may be used as a storage element for a single bit. At the (leading edge of) clock the J-K Flip-Flop configured below as a D flip-flop will assume (store) the input Boolean value (the S and R inputs are used to preset the flip-flop to a fixed initial Boolean state, if so-desired).

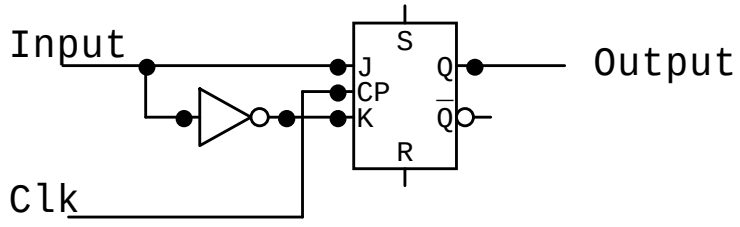

Figure 2.1: Implementation of a D Flip-Flop for 1 bit of memory storage.

2.1 Serial-In Serial-Out Shift Registers

This storage element may be connected in tandem with other comparable stages to form a Serial-In Serial-Out Shift Register; upon each successive clock pulse the Boolean value stored in Stage ***y*** is transferred (shifted) to stage ***y+1***, and the next input is placed in Stage 1, as shown in Figure 2.2. At the end of ***N*** shifts, an ***N***-bit word resides in the register.

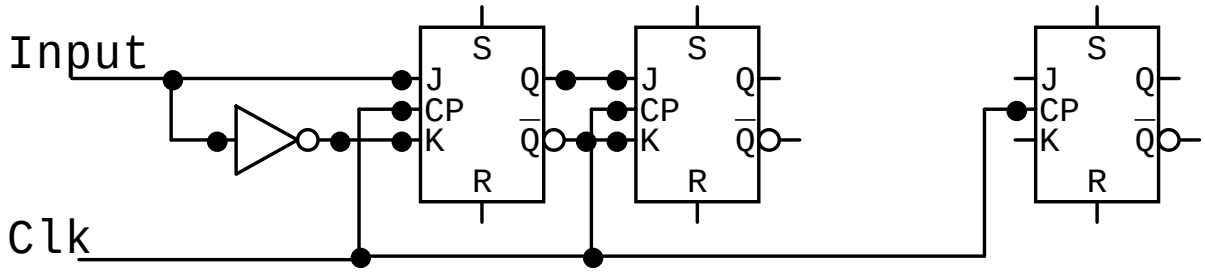

Figure 2.2: N-bit Shift Register using JK Flip-Flops

2.2 Parallel-In Parallel-Out Shift Registers

Opposed to loading data in serial, a Parallel-In Parallel-Out shift register loads the data into the shift register simultaneously for all bits by using parallel data lines into each of the D Flip-Flops. In a similar fashion, once each bit is stored in the register, all bits are available simultaneously as outputs using parallel output data lines, rather than on a bit-by-bit basis with the Serial-Out Shift Register, as shown in Figure 2.3.

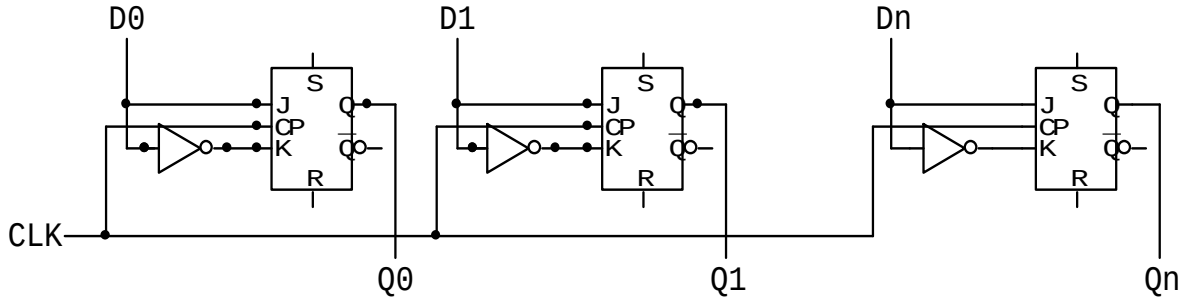

Figure 2.3: N-bit Parallel Shift Register using JK Flip-Flops

If data is loaded serially and read out in parallel, the Shift Register functions as a Serial-In Parallel-Out Shift Register. For data that is loaded in parallel and shifted out serially, the Shift Register functions as a Parallel-In Serial-Out Shift Register. More generally, shift registers may be configured to allow shifting of data to the right or to the left, as indicated

by the Bi-Directional Shift Register in Figure 2.4. Universal Shift Registers allow shifting of data in both the right and left directions, and may shift data in/out in serial or in parallel, thereby allowing them to act as Bi-Directional Serial-In Serial-Out, Serial-In Parallel-Out, Parallel-In Serial-Out, or Parallel-In Parallel-Out Shift Registers.

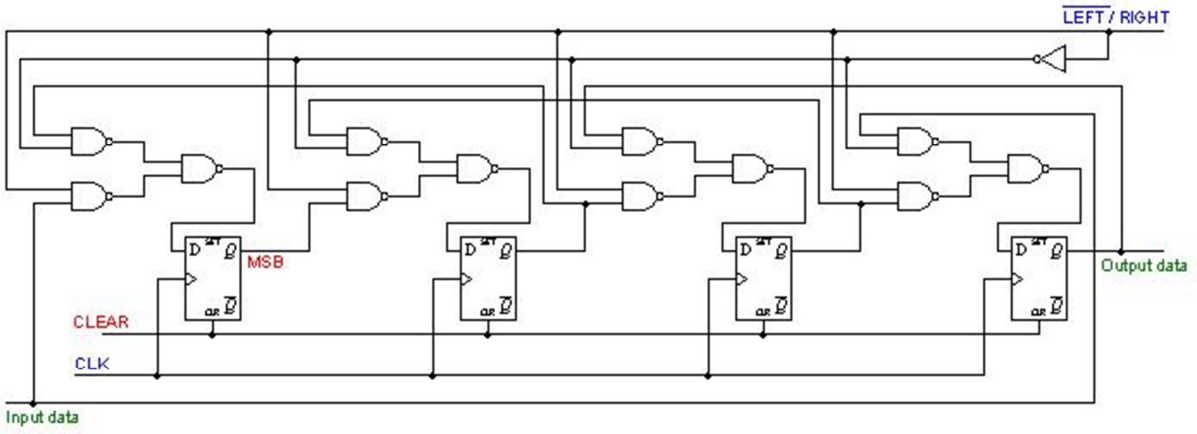

Figure 2.4: Bi-Directional Serial-In Serial-Out Shift Register

3. PRELAB

1. Design a 4-Stage Serial-In Serial-Out Shift Register using 74LS76 J-K flip-Flops. Structure your design so that the data is shifted (appears at the Q output of the next stage) on the leading edge of the clock. Use NAND gates for any required inverters. Note from the data sheet that the 7476 is a master-slave configuration. The data is moved into the master on the leading edge of clock and the flip-flop output (the slave) changes state on the trailing edge of clock.

2. Verify the 4-Stage Serial Shift Register using Multisim. Use a Clock Frequency of 1 Hz, and use a switch to manually toggle the input of the Shift Register to shift bits into the device. Use a digital Oscilloscope to examine the output waveform of the Shift Register.

3. Design a 4-Stage Bi-Directional Serial-In Serial-Out Shift Register using 74LS76 J-K Flip-Flops and NAND Gates. Structure your design so that the data is shifted on the leading edge of the clock.

4. Verify the 4-Stage Bi-Directional Serial-In Serial-Out Shift Register using Multisim. Use a Clock Frequency of 1 Hz, and use switches to manually toggle the inputs of the Shift Register to shift bits into the device. Use a digital Oscilloscope to examine the output waveforms of the Shift Register.

5. LAB ASSIGNMENT

5.1 Serial-In Serial-Out Shift Register

1. Construct your 4 Stage Serial-In Serial-Out Shift Register. Connect a Logic Bit Input Momentary Contact Switch as the Clock Input, and one Logic Bit Input Switch as your Data Input. Use Logic Bit Output LED's to display the output (Q) of each of the four stages. As the flip-flops' clock inputs require more drive than is available from the Momentary Contact Switch (directly connected), connect the output of this switch first to a type 14 Inverter (which will be used as a "buffer") and the output of this buffer to the clock inputs to the flip-flops.

2. Connect a second Logic Bit Input Switch as an external Clear for all stages of the Shift Register. Connect the Preset input of each of the stages so that the Preset function is disabled. In practice the Preset and Clear inputs to each Flip-Flop, if not used in the circuit, should be connected in a comparable fashion (so that the function is permanently disabled).

3. Turn On the power. Reset the Shift Register (all stages at Q = 0) with the external Clear Input. Call this (Shift Register) State Zero (0).

    A. With the Logic Bit Input Switch, set the Data Input HIGH. Depress (and release) the Momentary Contact Switch to form a Clock Pulse. Observe the Q output of each of the Flip-Flops. Call this State 1.

    B. Repeat 6A for the input LOW. Call this State 2.

    C. Repeat 6A for the input LOW. Call this State 3.

    D. Repeat 6A for the input HIGH. Call this State 4.

    E. Labeling the stages S1, S2, S3 and S4, S1 being connected to the Data Input, complete the following table.

State	Input	S1	S2	S3	S4
State 0	**None**				
State 1					
State 2					
State 3					
State 4					

5.2 Bi-Directional Serial-In Serial-Out Shift Register

1. Modify your circuit to construct a 4-Stage Bi-Directional Serial-In Serial-Out Shift Register. Use NAND Gates as necessary for the SOP terms needed to implement the Bi-Directional Shift Register, as indicated in Figure 2.4. Note that you will have

to add inverters to the output of each SOP term to interface with the K inputs of the J-K Flip Flops. The J inputs should be left non-inverted. See Figure 2.3 as an example of how to implement a series of D Flip-Flops using J-K Flips Flops.

2. Connect an additional Logic Bit Input Switch to create the Toggle Input between the Shift Right and Shift Left operations.

3. Repeat Part 3 of Section 5.1, first holding the Toggle Input HIGH. Then repeat the process a second time holding the Toggle Input LOW. Verify the Shift RIGHT and Shift LEFT operations for State 0 – State 4.

5. REVIEW QUESTIONS

1. Can S-R latches be used to create D Flip-Flops? If so, how?

2. What is the difference between the Serial-In Serial-Out, Serial-In Parallel-Out, Parallel-In Serial-Out, and Parallel-In Parallel-Out Shift Registers?

3. How many Shift Register stages are required to store a 16-Bit Binary Number?

4. What devices would you use to interface a 16-Bit Binary Number to a Serial-In Serial-Out Shift Register at the Input and Output of the Register?