ECE 85L Digital Logic Design Laboratory

Fresno State, Lyles College of Engineering
Electrical and Computer Engineering Department

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Laboratory 13 – Counters

1. OBJECTIVES

- Understand the Basic Operation of a Counter
- Simulate, Fabricate, and Test a 4-Stage Ring Counter
- Fabricate and Test a 4-Stage Binary Counter

2. DISCUSSION

2.1 Counters

A counter is a circuit comprised of an interconnection of Flip-Flops (and perhaps other combinatorial circuitry) that implements a particular state diagram which is called the counting sequence. The input to a counter is called a "Clock". Since one Flip-Flop has two states, a minimum of ***N*** Flip-Flops is required to implement any counting sequence ranging from 0 to 2_{N-1} counts.

Counters are classified as:

- **Synchronous –** if each stage is clocked
- **Asynchronous –** if only the first stage is clocked.

The counting sequence may be:

- **Up –** 0, 1, 2, 3, ...
- **Down –** 8, 7, 6, ...
- **Random –** 5, 3, 8, 4, ...

In addition the counter may be:

- **Repetitive –** 0, 1, 2, 3, 0, 1, 2, 3, ...
- **Non-Repetitive –** 5, 4, 3, 2, 1, (STOP)

And finally the counter may be:

- **Self-Starting –** Turn on the power and the counting sequence begins.
- **Non Self-Starting –** Some initialization step is required to initiate the counting sequence.

We will look at two quite different counters in this laboratory: the Ring Counter and the Binary (Ripple) Counter.

2.2 Ring Counters

Ring Counters form a class of divide-by ***N*** circuits; the Ring Counter is formed with a serial Shift Register and feedback.

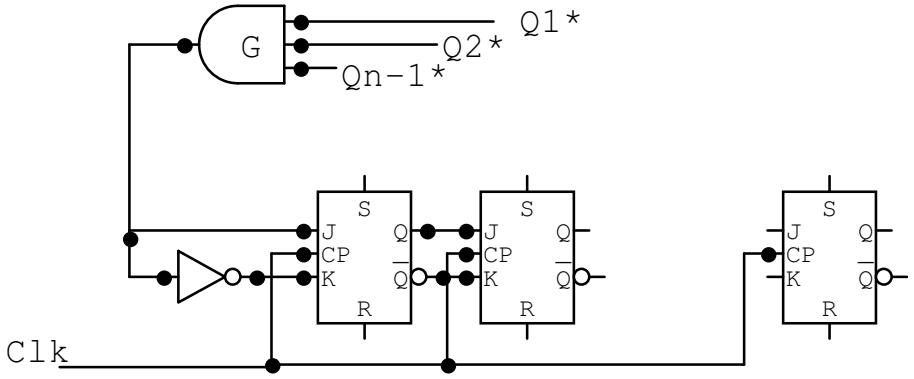

Figure 2.1: Implementation of a Ring Counter using a Shift Register and Feedback

Stage 1, driven by **AND** gate ***G***, will be continually fed with 0's which in turn will be propagated (shifted) into the other Stages until such time as all outputs from Stages 1 to ***N*** have 0's in them. At this point gate ***G*** is enabled and a 1 is inserted in Stage 1 at the next clock cycle. The 1 in Stage 1 disables gate ***G***. The 1 is shifted along the register with each subsequent clock cycle until it resides in Stage ***N***. At this point ***G*** again is enabled and the 1 is "re-circulated" (conceptually shifted out of Stage ***N*** and into Stage 1). Since each stage of the counter is clocked, the Ring Counter is Synchronous.

2.3 Binary (Ripple) Counters

When connected as a T Flip-Flop with the J and K inputs tied to $\mathbf{V_{cc}}$ (Logic 1), the J-K Flip-Flop will change State each alternating clock cycle.

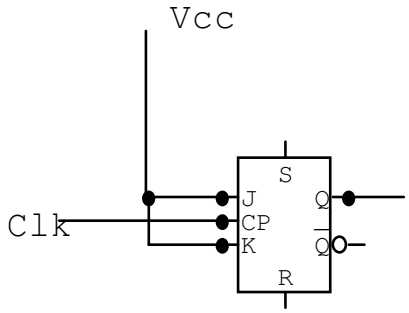

Figure 2.2: Implementing a T (Toggle) Flip-Flop from a J-K Flip Flop

The output ***Q*** is itself a Clock of twice the Period (half the Frequency) of the original Clock. Hence the Flip-Flop is said to be a Divide-by 2.

Such Flip-Flops can be connected in tandem to form a Binary Counter (a so-called ripple counter) where the output of the N^{th} stage is the original clock divided by ***2N***. Since only the first stage of this counter is clocked, the remaining stages each change as a result of changes in preceding stages. Changes are said to "ripple" from left to right. As such the Binary (ripple) counter is Asynchronous.

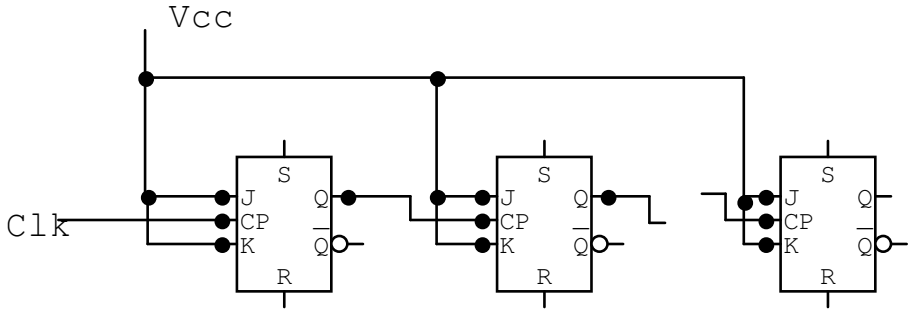

Figure 2.3: Implementation of a Ripple Counter using J-K Flip Flops as T-Flip Flops

3. PRELAB

1. Modify the 4-Stage Shift Register from the previous lab to design a 4-Stage Ring Counter. Use a 74LS40 4-Input NAND Gate a 74LS04 Hex Inverter to implement any required AND and NOT operations. Simulate the circuit using Multisim, and examine the output waveforms from each of the J-K Flip Flops to verify the ring oscillation of the circuit.

2. Create a 4-Stage Ripple counter using J-K Flip Flops. Simulate the circuit using Multisim, and examine the output waveforms from each of the J-K Flip Flops to verify the counting operation of the circuit.

4. LAB ASSIGNMENT

4.1 Ring Counter

1. Construct the 4-Stage Ring Counter Circuit using J-K Flip Flops and the 74LS40 and 74LS04 chips. Use a Function Generator with a Frequency of 10 kHz as a Clock (CLK) Input. Be sure to verify the TTL logic levels of the CLK signal **before** hooking it up to your circuit.

2. Draw the waveforms for the CLK and each of the Outputs ***Q*** from each of the Stages S1 – S4 of the Ring Counter (2 at a time). Make sure you draw the correct phase relationships between the ***Q*** outputs. To assist in this process, it is useful if you trigger the oscilloscope off the ***Q*** output of one of the stages for all observations.

3. Connect the ***Q*** output from each of the 4 Flip-Flops to one of the Logic Bit Output LEDs. Lower the frequency of the CLK to approximately 1 Hz and observe the timing sequence as displayed by the 4 LEDs.

4. Demonstrate your working circuit to your Instructor.

4.2 Binary Ripple Counter

1. Construct the 4-Stage Binary Ripple Counter using J-K Flip Flops. Connect the Counter Input (CLK) to a Square Wave Input with a Frequency of 10 kHz from the Function Generator. Again, verify the TTL levels of the CLK signal **before** hooking it up to your circuit.

2. Labeling your counter stages as A, B, C, and D (with the input of Stage A being connected to the CLK), connect a NAND gate to form an Output X which is LOW when:

   A = 1 (i.e., the Output Q from Stage A is HIGH)
   B = 0
   C = 0
   D = 1

   This output detects when the counter is in Decimal State 9.

3. Observe the outputs of all 4 counter stages (two at a time) on the oscilloscope (Hint: Triggering off the lowest frequency signal will ease this process). Draw waveforms for the CLK, A, B, C, D, and X. Below these waveforms label each of the combinations (Counter States) A, B, C, and D with the Binary and Decimal equivalent (e.g., A = 0, B = 0, C = 1, D = 1 corresponds to Binary 1100, or Decimal 12).

4. Connect each of the 4 Flip-Flop outputs A, B, C, and D, as well as X to a Logic Bit Output LED. Adjust the frequency of the CLK to approximately 1 Hz. Verify the operation of the counter by observing the counting sequence displayed on the LEDs.

5. Demonstrate your working circuit to your Instructor.

Extra Credit

Use a 7-Segment Decoder and 7-Segment Display to verify the decimal operation of the counter by feeding the A, B, C, and D outputs for the counter into the 7-Segment Decoder. Adjust the NAND gate output X to detect an output of Decimal 10, which should then be used to Reset each of the Flip-Flops, so the Ripple Counter only counts between Decimal 0 – 9.

5. REVIEW QUESTIONS

1. How many ripple counter stages are required for a divide by 128 circuit?

2. When observing a Binary Counter Circuit on the Oscilloscope, why is it advisable to trigger off the lowest (counter) counter frequency signal?

3. Why are J-K Flip-Flops used rather than R-S Flip-Flops in a Binary Counter?

4. Can a Ring Counter be designed to count by any (not necessarily divisible by 2) number?

5. Compare the number of components required for a Divide-by-16 circuit implemented with a Ring Counter compared to being implemented with a Binary Counter with gates to decode the Flip-Flop outputs.

6. Is the Ring Counter self-starting? Why?