

California State University, Fresno
Department of Electrical and Computer Engineering

ECE 90L Principles of Electrical Circuits Laboratory
Experiment No. 8: Operational Amplifier Circuits

Objective

In this experiment you will make three op-amp circuits: a unity-gain buffer amplifier, a weighted summer, and a difference amplifier.

Prelab

For an op-amp circuit with negative feedback we can use the flow chart of Figure 1 to find the output voltage v_0 .

Unity-Gain Buffer Amplifier

A unity-gain buffer amplifier is shown in Figure 2. This is an example of an op amp with negative feedback, and we can use the flow chart of Figure 1 to find how the output v_0 is related to the input v_i . We assume that the voltage at the inverting input equals the voltage v_i at the non-inverting input. Since the output is connected to the inverting input via a simple conductor, $v_0 = v_i$. This will be true as long as the *output* lies between the rails ($-V_{\text{rail}} < v_0 < V_{\text{rail}}$). We can also say that $v_0 = v_i$ as long as the *input* lies between the rails ($-V_{\text{rail}} < v_i < V_{\text{rail}}$). Since the output follows the input, as long as the input lies between the rails, this circuit is also called a *voltage follower*.

You might think that this circuit is useless, that we can also achieve $v_0 = v_i$ with a stand-alone conductor, no need for an op amp. But the unity-gain buffer amplifier of Figure 2 has an important feature that a stand-alone conductor does not. The unity-gain buffer amplifier draws no current from any source connected to its input; whereas a simple conductor would draw current (as long as there is a complete circuit). Consider the following example.

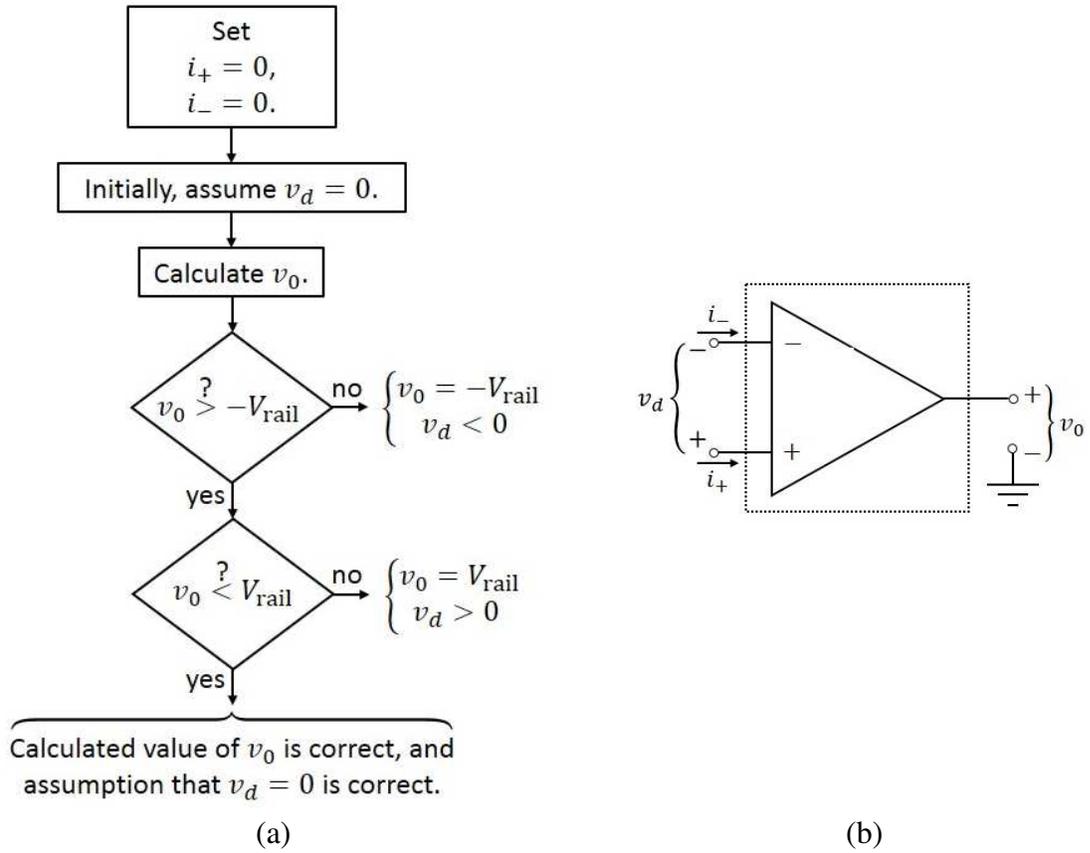


Figure 1: (a) Flow chart for analysis of op-amp circuit having negative feedback, and (b) definitions of the variables i_+ , i_- , v_d , and v_0 .

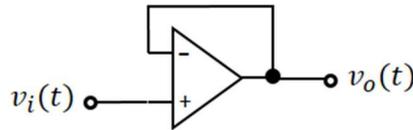


Figure 2: Unity-gain buffer amplifier

We have an electronics module that includes a source. We will be connecting the output of this module to a load. We will use different loads on different occasions. The situation is shown in Figure 3, where the module is modeled by its Thévenin equivalent, having a Thévenin source V_{Th} and an output impedance R_{Th} (which is real in this case, and therefore a resistance). The load is modeled as the resistance R_L . We will be using different loads. R_L has, in general, a different value for each new load. We would like the voltage V_L appearing across R_L to always be the same, regardless of load. This is a common application.

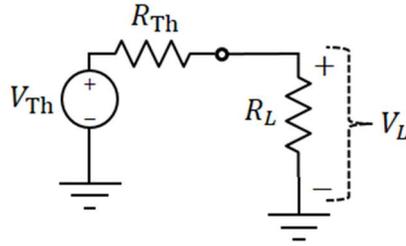


Figure 3: Thévenin equivalent of electronics module with load attached

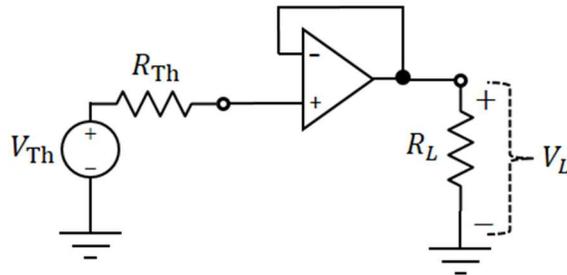


Figure 4: Unity-gain buffer amplifier isolates the module from the load.

With the circuit of Figure 3, V_L results from a voltage division:

$$V_L = \frac{R_L}{R_L + R_{Th}} \cdot V_{Th}.$$

When the load is replaced with a different one having a different value for R_L , the load voltage V_L changes. This is not what we want.

Consider instead the circuit of Figure 4. A unity-gain buffer amplifier has been inserted between the electronics module and the load. The unity-gain buffer amplifier draws no current from the module, so there is no voltage drop across R_{Th} . The voltage V_{Th} appears at the non-inverting input of the op amp and at the output of the op amp. Therefore,

$$V_L = V_{Th}.$$

This assumes that $-V_{rail} < V_{Th} < V_{rail}$. The load voltage V_L is independent of the load.

The unity-gain buffer amplifier is sometimes called an *isolation amplifier* to emphasize the fact that this circuit isolates the electronics module (which has been modeled as a Thévenin equivalent circuit) from the outside world. By isolation is meant that the outside world draws no

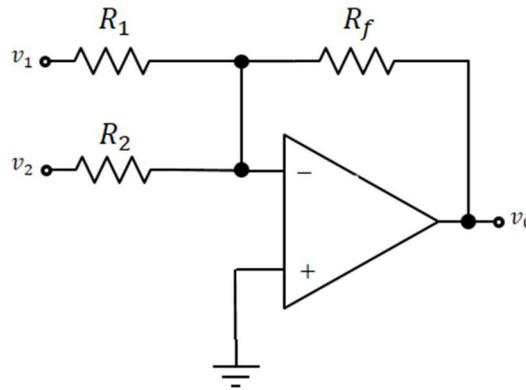


Figure 5: Weighted summer

significant current from the module. And this isolation is enforced even as the isolation amplifier manages to sense the voltage V_{Th} .

Where does the current come from that passes through the load in the circuit of Figure 4? It certainly doesn't come from V_{Th} . When V_L is positive, current flows from the V^+ DC source (not shown in Figure 4), through the op amp to its output terminal, and through the load to ground. When V_L is negative, current comes out of ground, passes through the load, enters the op amp through its output terminal, and then enters the V^- DC source (not shown in Figure 4). Upon leaving the V^- DC source, the current passes to ground, completing the circuit.

Weighted Summer

A weighted summer is shown in Figure 5. This circuit's output voltage v_0 is a function of two input voltages: v_1 and v_2 . This circuit has negative feedback and can be analyzed using the flow chart of Figure 1.

Exercise: For the weighted summer of Figure 5, find an expression for the output v_0 as a function of the inputs v_1 and v_2 . (The parameters R_1 , R_2 and R_f should also appear in your expression.) You only need to consider the case where $-V_{rail} < v_0 < V_{rail}$.

Design a weighted summer that implements the following formula:

$$v_{out} = -v_1 - 2 v_2$$

where v_1 and v_2 are inputs and v_{out} is the output. Use a 15-k Ω resistor in the feedback path of the circuit.

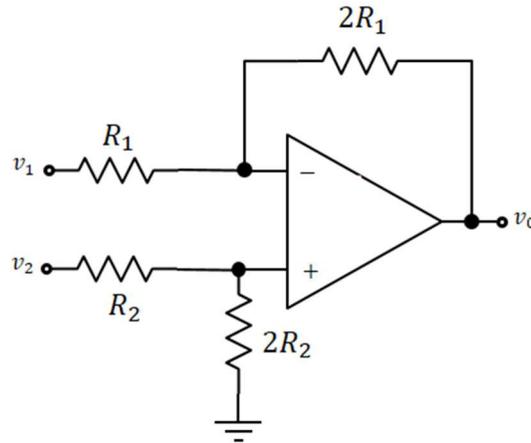


Figure 6: Difference amplifier

Difference Amplifier

A difference amplifier is shown in Figure 6. This circuit's output voltage v_0 is a function of two input voltages: v_1 and v_2 . This circuit has negative feedback and can be analyzed using the flow chart of Figure 1.

Exercise: For the difference amplifier of Figure 6, find an expression for the output v_0 as a function of the inputs v_1 and v_2 . (The parameters R_1 and R_2 should also appear in your expression.) You only need to consider the case where $-V_{\text{rail}} < v_0 < V_{\text{rail}}$.

Procedure

Place an LM741 op amp on the solderless breadboard. The pin-out of this op amp is illustrated in Figure 7.

Configure the Siglent DC power supply to be the source of +12 V for pin 7 and -12 V for pin 4. But do not apply live voltages to the op amp until ready to make measurements. Set the maximum current to 0.2 A for both sources. Place the DC power supply in series mode. Set the CH1 voltage to 12 V, causing the CH2 voltage to be 12 V also. Connect the CH2 - terminal, which is internally connected to the CH1 + terminal while in series mode, to ground. With this configuration, the CH2 + terminal is at +12 V relative to ground and the CH1 - terminal is at -12 V relative to ground.

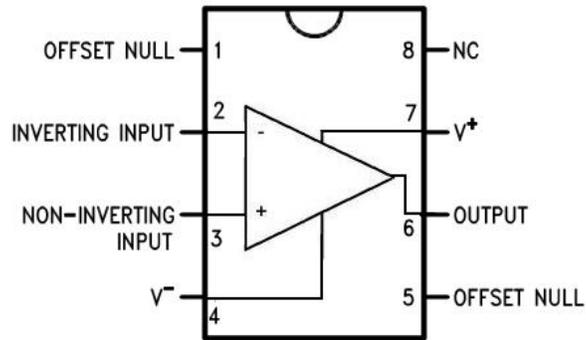


Figure 7: LM741 pin-out

Unity-Gain Buffer Amplifier

Build the circuit of Figure 3. Here you are recreating a module (modeled as a Thévenin equivalent circuit) that is connected directly to a load. For V_{Th} use the Siglent power supply's third source, set for 5 V. For R_{Th} use a 1.0-k Ω fixed (color-coded) resistor. For R_L use a precision, adjustable resistance from a resistance decade box.

You will be setting R_L to several different values, but R_{Th} will remain 1.0 k Ω . Use the following 3 values for R_L : 1.0 k Ω , 3.0 k Ω , and 9.0 k Ω . For each value of R_L , record V_L .

Now insert a unity-gain buffer amplifier (using the LM741 op amp) between the module and the load, as shown in Figure 4. Don't forget to turn on the DC supply voltages for the op amp. With $V_{Th} = 5$ V and $R_{Th} = 1.0$ k Ω (as before), record V_L as a function of R_L for the following values of R_L : 1.0 k Ω , 3.0 k Ω , and 9.0 k Ω .

In the circuit of Figure 4, for which the module is connected to the load through an isolation amplifier, replace the $V_{Th} = 5$ V source with the synthesized frequency generator. Set the generator to produce a 1-kHz sinewave with an amplitude of 5 V. As before, $R_{Th} = 1.0$ k Ω . Set R_L to 1.0 k Ω . Observe the output of the synthesized frequency generator on channel 1 and V_L on channel 2 of the oscilloscope. Take a picture of the oscilloscope display.

Weighted Summer

Select the resistors that you will need for the weighted summer that you designed. Measure and record the resistances.

Construct the weighted summer. Set the synthesized frequency generator to produce a 1-kHz sinewave having an amplitude of 1 V. Adjust the offset of the synthesized frequency generator to minimize the DC bias.

Before applying the output of the synthesized frequency generator to the weighted summer, pass the generator's signal through a 0.2- μ F capacitor. The purpose of this capacitor is to block any remaining DC bias in the synthesized frequency generator's output.

For each row in Table 1, observe the output of the synthesized frequency generator on channel 1 and the output of the weighted summer on channel 2. Also for each row, measure the RMS voltage of the synthesized frequency generator output and of the weighted summer output. As an example of how to interpret Table 1, the first row of numbers suggests that you should apply the synthesized frequency generator to v_1 and you should connect v_2 to ground.

Table 1: Amplitudes for v_1 and v_2 for the weighted summer

v_1 amplitude (V)	v_2 amplitude (V)
1.0	0
0	1.0
1.0	1.0

Difference Amplifier

Build the difference amplifier of Figure 6. Use fixed (color-coded) resistors. $R_1 = 1.5 \text{ k}\Omega$ and $R_2 = 1.5 \text{ k}\Omega$. Therefore, the resistor labeled $2R_1$ will be 3.0 k Ω , and the resistor labeled $2R_2$ will be 3.0 k Ω . Before making measurements, don't forget to turn on the DC supply voltages for the op amp.

You will test the difference amplifier with DC inputs. You will use the Siglent power supply's third source, set for 5 V, for this purpose. Table 2 summarizes the three tests that you should perform with the difference amplifier. For each row in Table 2, measure v_0 .

Table 3: DC inputs v_1 and v_2 for difference amplifier

v_1 (V)	v_2 (V)
5.0	0
0	5.0
5.0	5.0

Lab Report

Explain one situation where the unity-gain buffer amplifier is useful.

In the weighted summer you built, the weighting coefficients are negative. Explain how you could build a weighting summer with positive coefficients. (You are allowed to use more than one op amp.)

Is it necessary for one of the input terminals of the difference amplifier to be grounded?

As usual, you should compare measurements with expectations.